Micro-RDC

Microelectronics Research Development Corporation

Radiation-Hardened-By-Design Structured ASIC

Feature Sheet

Single-Layer Configurable Design-Hardened Structured ASIC Features:

- IBM 9LP (Low Power) 90nm CMOS technology, processed on IBM's "Trusted" fabrication line (on shore)
- Design-Hardened Fabric w/Distributed Dual Port SRAM (Logic Cell w/Memory in Each Tile)
- Logic uses selectable 1ns and/or 2ns delay, patented Temporal Latch structures to provide SEU Immunity
- Radiation Tolerance of Logic & Memory: TID > 3Mrad(Si), SEU < 1e-8 to 1e-10 Errors/bit-day, SEL > 75 MeV-cm^2/mg (LET)
- Design-Hardened PLL, Input Frequency: 10MHz to 125MHz
- Design-Hardened 1.25 Gb/s LVDS TX/RX I/O; Input Frequency: 75 MHz to 125 MHz
- Design-Hardened 8K X 8 Blocks of Configurable SRAM w/EDAC
- Each Die Contains Design-Hardened Via-Configurable (Boot-up) ROM
- Design-Hardened Via-Configurable General Purpose I/O
- Dual Voltage Supply; 1.2V core and 1.8V to 2.5V I/O
- Ultra-Low Power (Only 10s to a few 100s of mWs per design)
- On-chip Health (Temperature) Monitors
- Some Die can be configured for COMSEC Applications

DESIGN MACROS NOW AVAILABLE

Multi-Project-Wafer Reticles will be Fabricated Containing 4 Different Die Sizes, Providing 6 Different Feature Sets:

Die Size (mm²)	User Die / Reticle	CMOS User I/O	LVDS* I/O	Equivalent Logic Gates	Flip Flops	Distributed DP SRAM Memory	Block Memory SRAM w/EDAC	VROM	PLLs
~ 3 X 3 (LO)	4	96	None	~104K	4,864	~76K Bits	None	4 X 9K bits X 8 (288K Bits)	None
~ 5 X 5 (FF)	1	118	4 Pair TX/RX	~173K	8,064	~126K Bits	5 Blocks 8K X 8 / Block	4 X 9K bits X 8 (288K Bits)	1 PLL
~ 5 X 5 (LO)	2	158	None	~286K	13,312	~208K Bits	None	4 X 9K bits X 8 (288K Bits)	None
~ 7 X 7 (EM)	1	248	None	~220K	10,240	~160K Bits	32 Blocks 8K X 8 / Block	4 X 9K bits X 8 (288K Bits)	None
~ 7 X 7 (FF)	1	192	8 Pair TX/RX	~478K	22,272	~348K Bits	8 Blocks 8K X 8 / Block	4 X 9K bits X 8 (288K Bits)	1 PLL
~ 10 X 10 (FF)	1	256	16 Pair TX/RX	~1.14M	52,992	~828K Bits	12 Blocks 8K X 8 / Block	4 X 9K bits X 8 (288K Bits)	2 PLLs
(LO) = Logic Only; (FF) = Full Feature; (EM) = Extra Memory									
* LVDS lanes are powered separately from the chip's core power, enabling use for COMSEC or for Trusted Keys.									

Initial Package Offerings*:

Die Sizes	Number of Pins					
~3mm X ~3mm	132 CQFP		181 PGA			
~5mm X ~5mm	132 CQFP	172 CQFP	181 PGA	208 CQFP	240 CQFP	
~7mm X ~7mm				208 CQFP	240 CQFP	255 LGA/CGA	484 LGA/CGA
~10mm X ~10mm					256 CQFP	484 LGA/CGA

* 1) Packages shown are for prototyping purposes.
  2) Custom packages for Flight can be developed. Note: A Custom 484 CLGA Package for Flight does exist for the 10mm x 10mm die

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The Cost of Obtaining Qualified ICs for Flight Programs is Greatly Reduced in Four Ways:

1) Using our design flow can result in <u>Reduced Design Hours/Design Cycle Time</u>. ViASIC's ViaPath place and route software converts a VHDL/Verilog design into a Design-Hardened Structured ASIC.
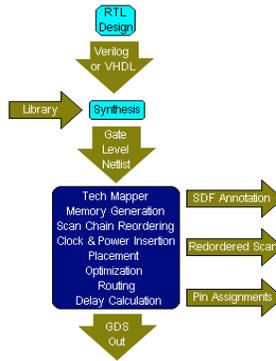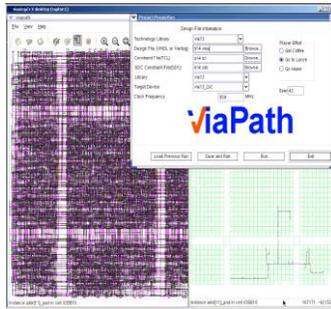
2) One-Layer Configurability Results in Fabrication <u>Costs Based on a Single Reticle Layer</u> (Via-3).

3) Multi-Project-Wafer Reticles Enable <u>Shared Reticle/Lot Fabrication Costs</u> Over Multiple Programs.

Typical Fabrication Lot Reticle Showing 10 Die Available
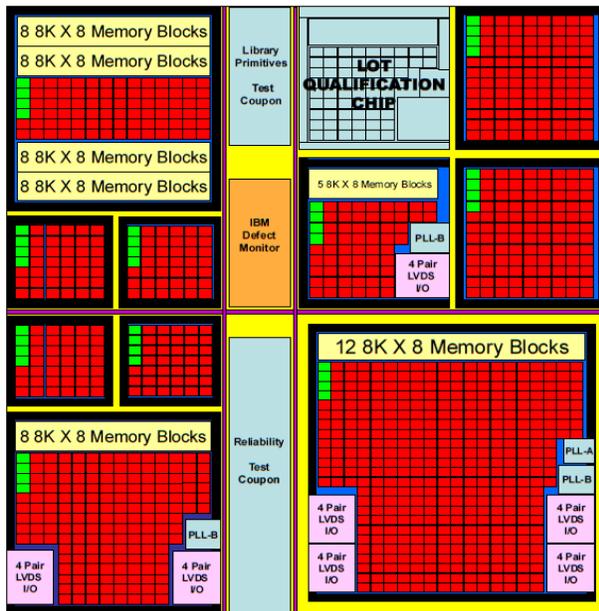
10 Die Available for Customer Personalizations:

4 = ~3mm X ~3mm die

3 = ~5mm X ~5mm die (2 Styles)

2 = ~7mm X ~7mm die (2 Styles)

1 = ~10mm X ~10mm die

4) A Lot Qualification Vehicle on every Reticle, enables Multi-Project-Wafers to <u>Share Flight Die Qualification Costs</u> for Multiple Programs.

A Low-Cost Solution for Low-Volume Radiation Hardened ICs

For more information, please contact:

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